**Digital System Design**

**BS(CE)-2k20**

**Semester Project Report**

**Traffic Control System**



**Submitted By:**

Abdullah Javed 20-CE-035

Ayesha Ehtisham 20-CE-038

**Submitted To:**

Engr. Fasih Ahmed

**Department of Computer Engineering**

**HITEC University Taxila**

Contents

[Introduction: 4](#_Toc137141056)

[Problem Scenario: 4](#_Toc137141057)

[Objective: 4](#_Toc137141058)

[Requirements: 5](#_Toc137141059)

[Tools Used: 5](#_Toc137141060)

[Major Design & Function Areas: 5](#_Toc137141061)

[Block Diagram: 6](#_Toc137141062)

[Truth Table: 6](#_Toc137141063)

[State Transition Table: 7](#_Toc137141064)

[Verilog Code: 8](#_Toc137141065)

[Flowchart: 13](#_Toc137141066)

[State Diagram: 14](#_Toc137141067)

[Conclusion: 14](#_Toc137141068)

**List of Figures**

[Figure 1 Lanes and Signals 4](#_Toc137141093)

[Figure 2 Block Diagram 6](#_Toc137141094)

[Figure 3 Verilog Code 8](#_Toc137141095)

[Figure 4 Flowchart 13](#_Toc137141096)

[Figure 5 State Diagram 14](#_Toc137141097)

**List of Tables**

Truth Table ………………………………………………………………………………………………………………………… 6

State Transition Table ……………………………………………………………………………………………………….. 7

**Traffic Control System in Verilog HDL**

# Introduction:

Our project scenario is that we have to develop a digital system which controls the flow of traffic on an intersection. This intersection has 4 lanes and each lane has a separate traffic signal. We need to develop a synchronous control system which controls all the signals.

# Problem Scenario:

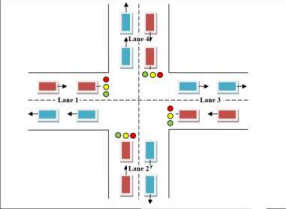


Figure 1 Lanes and Signals

# Objective:

The task is to design a state machine for a traffic control system for a 4 way road interchange, the state machine should follow the mentioned aspects of the system

1. Transitions must be in sequence, i.e. L1 -> L2 -> L3 -> L4

2. Resetting the system will bring the state machine to its *rst state,* where all the roads will be blocked until reset is released

3. Each Lane must get its **movement time** (*green lights on*)

4. Between each transition, there must be **clearance time** i.e. *red light* must be on for a short amount of time of both lanes

**5.** Lane 1 and Lane 3 are busy roads (main roads) so they should get larger **movements time** 6. Delay time for each light is given in the following table

# Requirements:

The following table describes the required time for each of the lanes for movement, stoppage and clearance:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Lane | Movement time (clock cycles) | Stop Time  (clock cycles) | Yellow Time (clock cycles) | Clearance Time (clock cycles) |
| L1 & L3 | 30 | 30 | 5 | 5 |
| L2 & L4 | 20 | 30 | 5 | 5 |

# Tools Used:

* EDA Playground
* Icarus Verilog Compiler
* GTK Wave
* Verilog HDL
* Lucid chart (For Flowchart and State Diagram)

# Major Design & Function Areas:

* Each State is given separate output
* Use of parameters
* Main logic is created with the help of case statement
* Assign method used for output
* External clock used for synchronous operation

# Block Diagram:

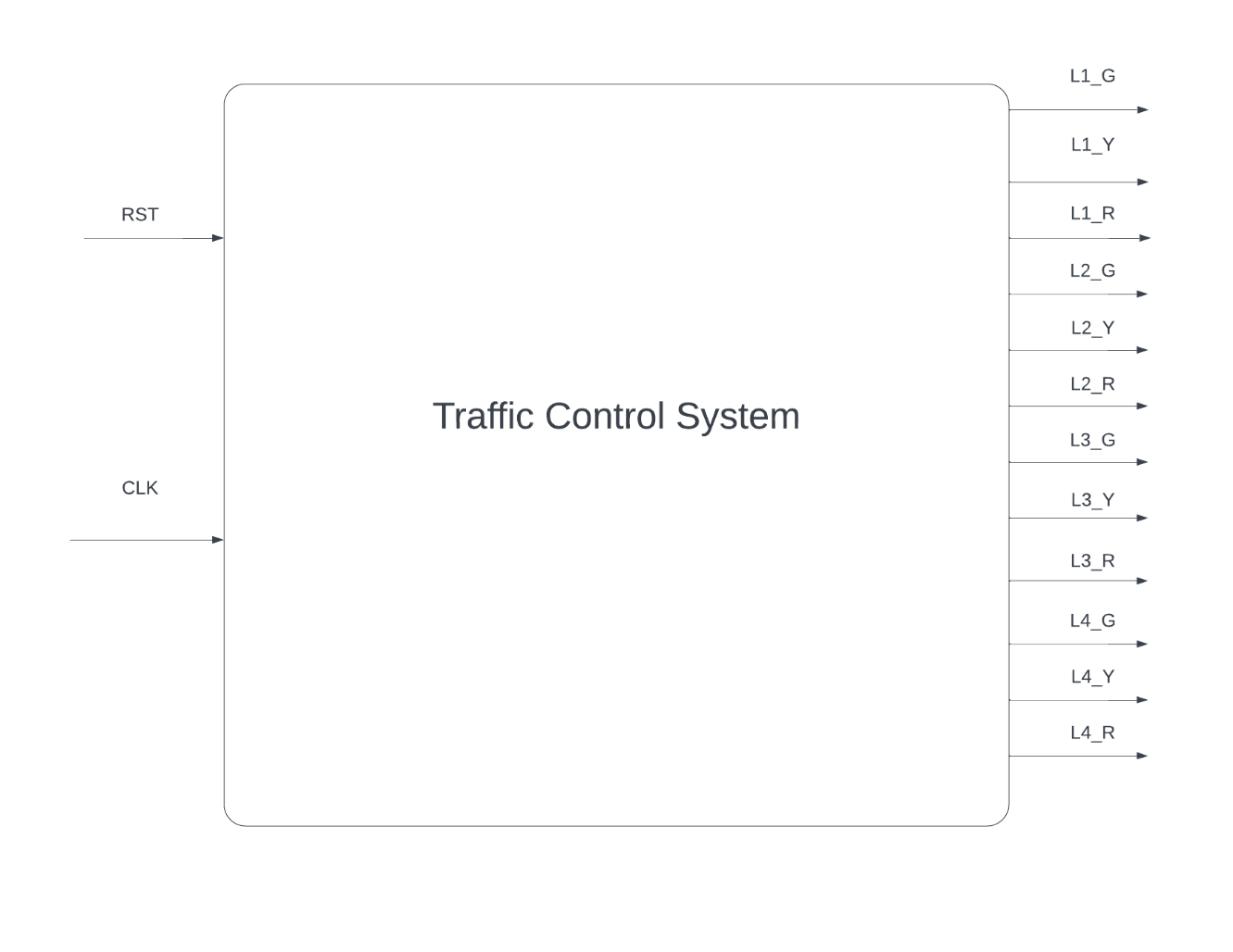


Figure 2 Block Diagram

# Truth Table:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **RST** | **CLK** | **L1\_G** | **L1\_Y** | **L1\_R** | **L2\_G** | **L2\_Y** | **L2\_R** | **L3\_G** | **L3\_Y** | **L3\_R** | **L4\_G** | **L4\_Y** | **L4\_R** |
| 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 2 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 3 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

# State Transition Table:

|  |  |  |
| --- | --- | --- |
| **Current State** | **Input** | **Next State** |
| L1\_G | 0 | L1\_Y |
| L1\_Y | 0 | L1\_R |
| L1\_R | 0 | L2\_G |
| L2\_G | 0 | L2\_Y |
| L2\_Y | 0 | L2\_R |
| L2\_R | 0 | L3\_G |
| L3\_G | 0 | L3\_Y |
| L3\_Y | 0 | L3\_R |
| L3\_R | 0 | L4\_G |
| L4\_G | 0 | L4\_Y |
| L4\_Y | 0 | L4\_R |
| L4\_R | 0 | L1\_G |

# Verilog Code:

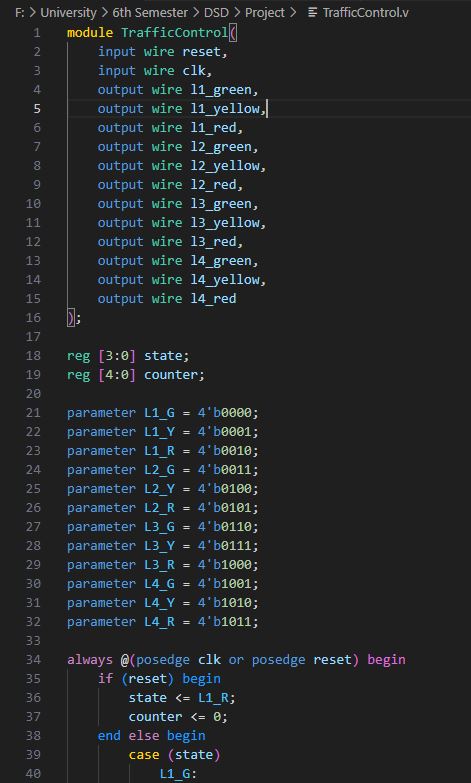
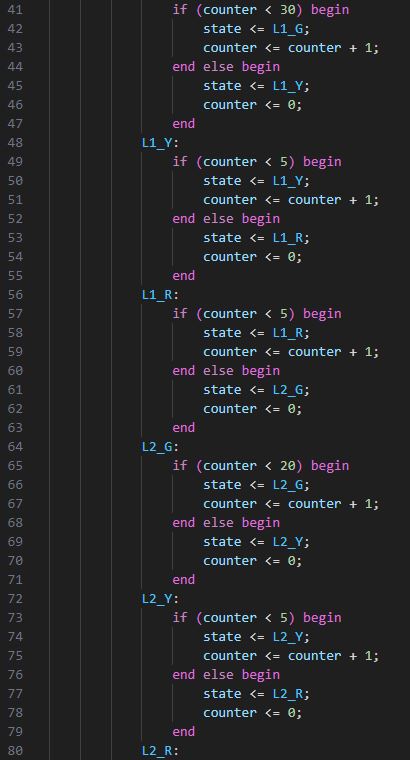
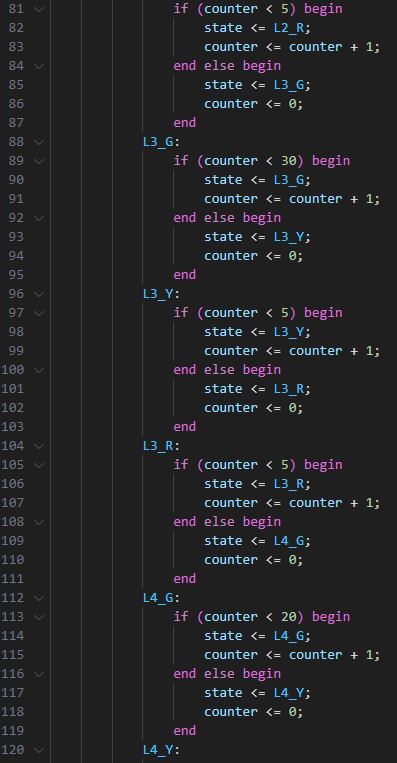
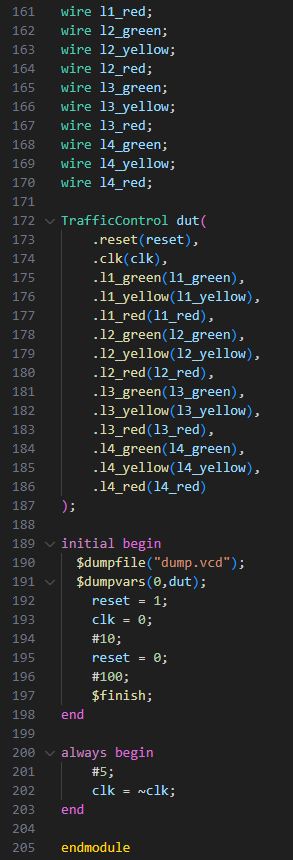


Figure 3 Verilog Code









# Flowchart:

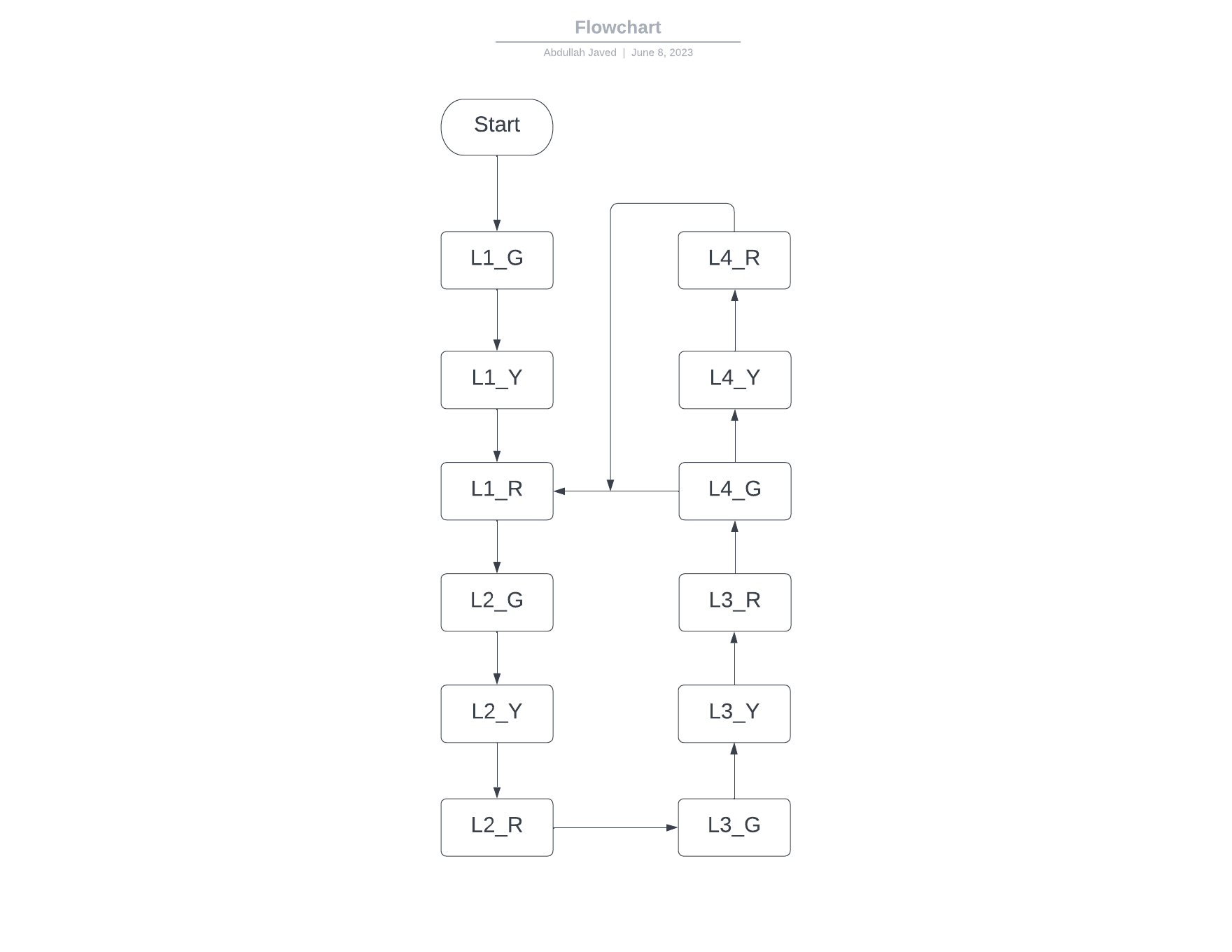


Figure 4 Flowchart

# State Diagram:

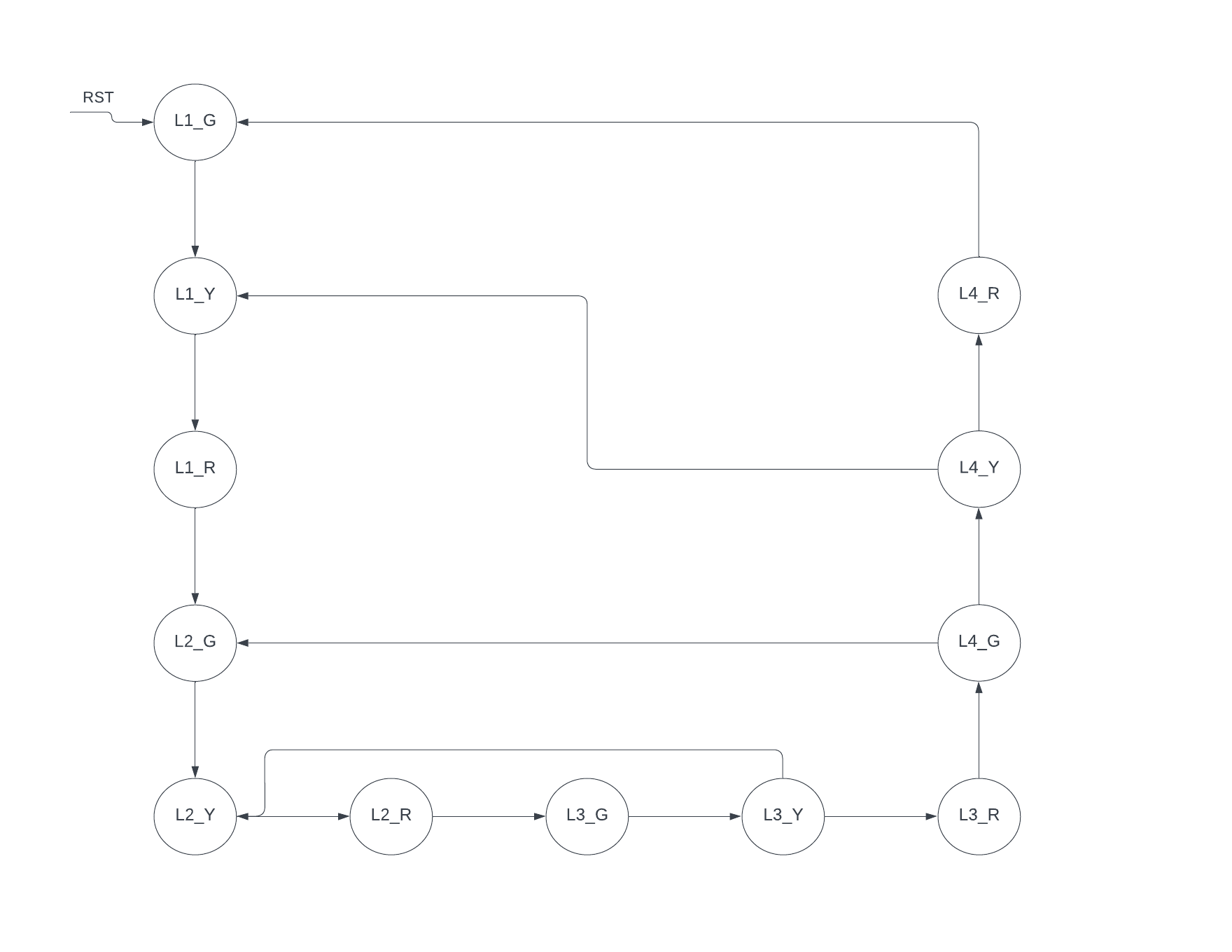


Figure 5 State Diagram

# Conclusion:

The outcome of the proposed system will be a fail-safe and fully functioning Traffic Control System. This system will be automatic, hence it will give movement time to each lane one by one, and will keep on repeating.